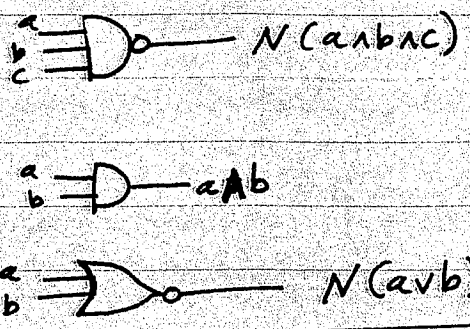
This shows that @ least one "result of pure logic design is in the literature.

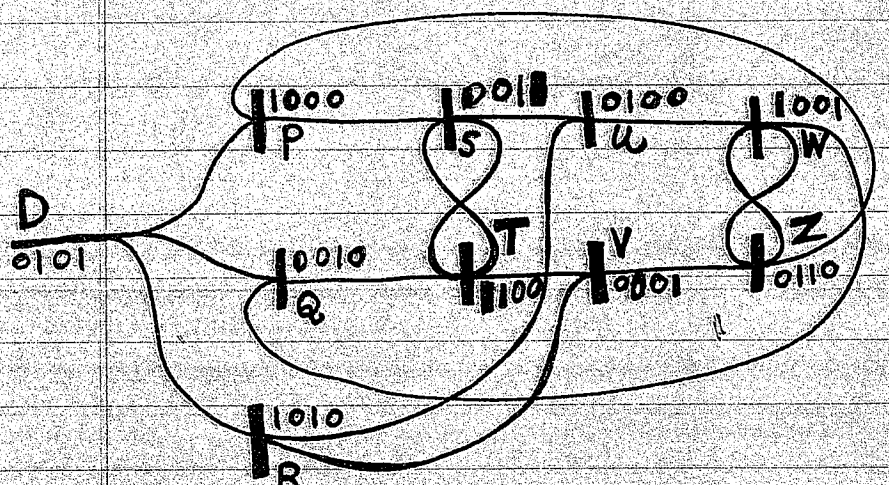


P, 59

J. R. Gibson
Electronic Logic Circuits
E. Arnold Pub. 1992
(1st pub 1979)

Diagram of Gibson's JK flip/flop without inputs except the "clock" D.

9/17 I call Gibson 9.17 since it has 9 markers & 17 leads.



D P Q R
P S
Q T
S T U
T S V
R U V
U W
V Z
W Z Q
Z W P

(See Gibson's circuit below. He uses NAND gates & this is equiv to LOT nor gates. On next page is 816 written for comparison.)

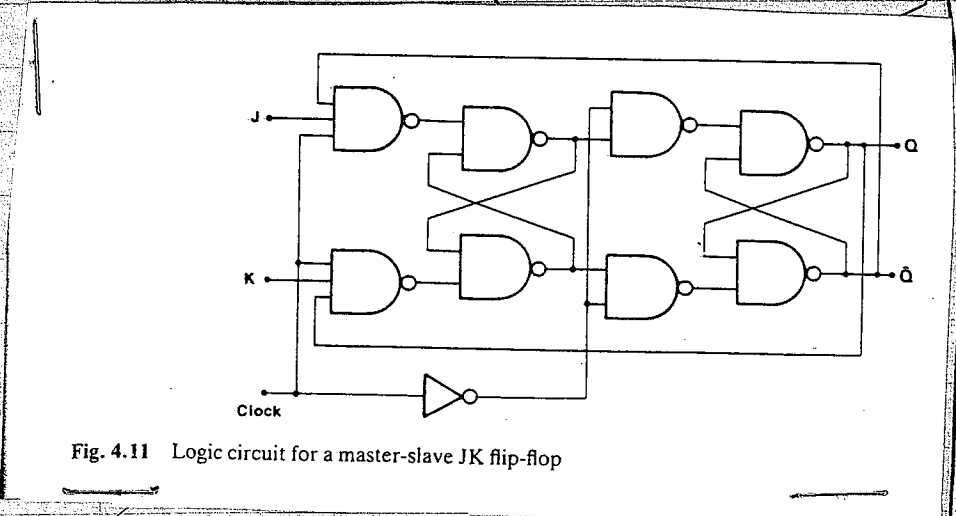
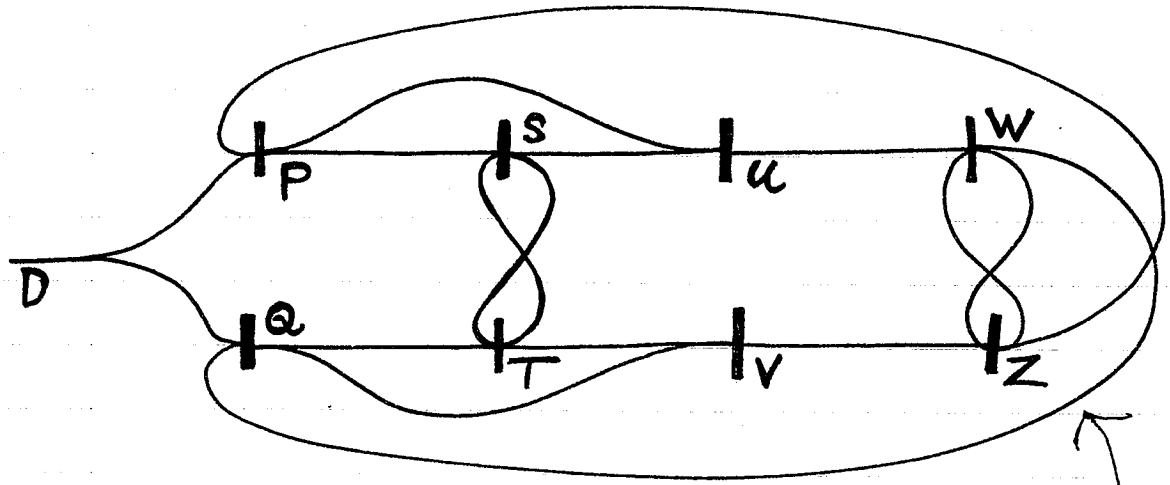
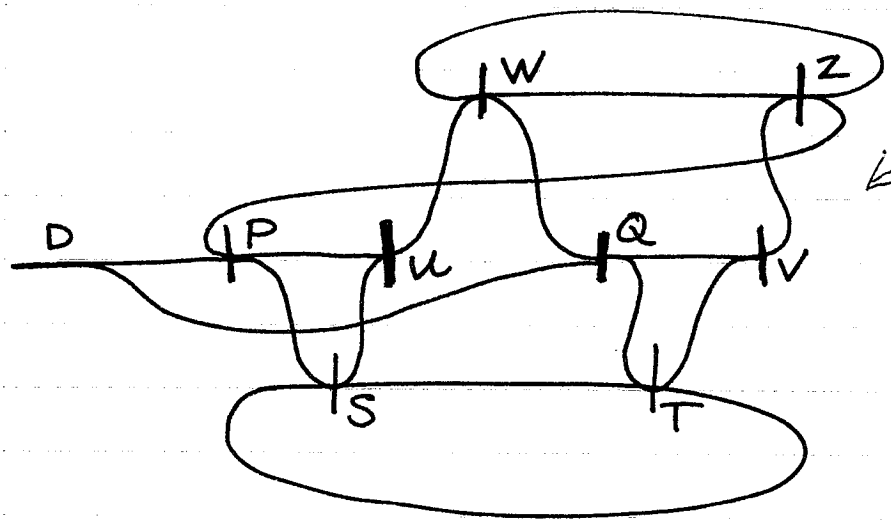


Fig. 4.11 Logic circuit for a master-slave JK flip-flop

D 0101 R 1010
P 1000
Q 0010
U 0100
V 0001
S 0011
T 1100
W 1001
Z 0110

alternate drawing of 816





These are both drawings of LOF 816.

Compare 816 with 917 on previous page and it is apparent that 816 is a more efficient form of 917. Both have extra leads to avoid race conditions. Both will operate correctly in the face of any choice of delay times for the markers.